

Masters of Power Solution

Product Brief

TSPAK, Innovative Top-Side Cooling Package



Target Applications





Key Features and Benefits of TSPAK

TSPAK LF version

- Top-side cooling package with an exposed drain at the surface, allowing direct heat dissipation to the heatsink.
- Offers superior thermal performance and supports high current capabilities.

TSPAK DBC version

- Integrates an isolated DBC ceramic pad on the surface, providing premium thermal performance and enhanced design flexibility.
- Features 3.6kV isolation voltage, extended creepage distance (5.23mm), and flexible mounting by directly connected to an external heatsink with thermal grease.

	Non-Isolated Design (LF version)	Isolated Design (DBC version)
Package		
Features	 Top-side cooling High heat spread effect Larger die size attachable than DBC version Design flexibility : Better Thermal Performance Comparable creepage distance (4.85mm) vs. Comp 	 Top-side cooling Isolated substrate / High dielectric strength Mounting flexibility with thermal grease Design flexibility : Better Thermal Performance Longer creenage distance (5.23mm) vs. Comp.

	 Industry standard package footprint (Pin-to-pin replacement) Kelvin source Package High temperature capability : T_{j (max)}= 175°C 	 Industry standard package footprint (Pin-to-pin replacement) Kelvin source Package High temperature capability : T_{j (max)}= 175°C
Benefits	 High current capability by thick wire bonding High power density : Smaller FOM factor Improved EMI and Easy to design Better thermal performance Lower switching losses 	 High current capability by thick wire bonding Easy inverter replace during repair Improved EMI and simplified design High power density : Smaller FOM factor Lower switching losses



https://www.powermastersemi.com

Power Master Semiconductor Co., Ltd

This innovative packaging leverages Power Master Semiconductor's latest generation of 1200V eSiC MOSFET (Gen2), employing cutting-edge technology to decouple a trade-off between specific on-resistance (R_{sp}) and short-circuit withstand time (SCWT). Compared to the previous generation, the new 1200V eSiC MOSFETs deliver 20% reduction in R_{DS(ON)} and a 15% improvement in SCWT, as well as a 45% reduction in switching losses

Performance Benchmark



Switching Performance

UIS Ruggedness (Avalanche current)



Short Circuit Withstand Time (SCWT)

20

POWERMASTER

25

Eoff _

30



TSPAK - 1200V Gen2 e/SiC MOSFET (Automotive Grade)

Package	TSPAK-LF Version	TSPAK-DBC Version
R _{DS(ON)_typ}		
21mΩ	PCRZ120N21M2A	PCR120N21M2A
40mΩ	PCRZ120N40M2A	PCR120N40M2A
60mΩ	PCRZ120N60M2A	PCR120N60M2A

HEADQUATERS

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